ADAS électronique

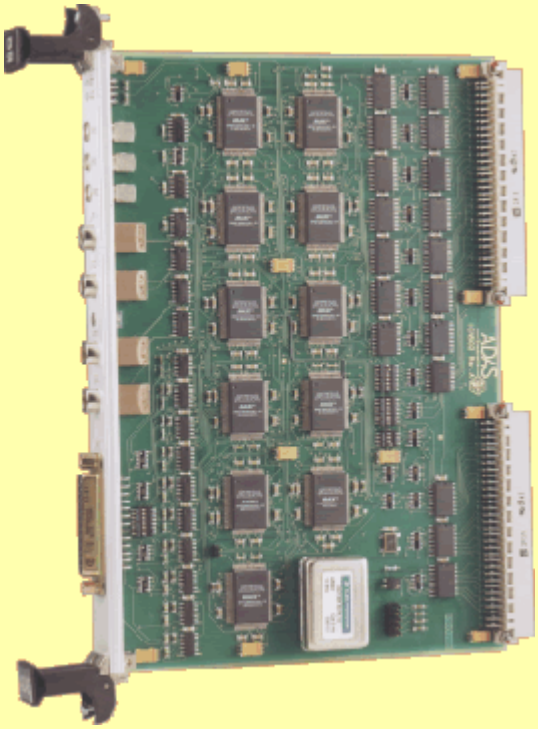
STB BCI Cables

# SYNCHRONIZED DDS GENERATOR FOR ISOCHRONOUS CLOCKS

# ICV 502

## Features

- GPS external reference PPS and 10MHz
- Internal reference by high precision, thermostatically controlled, oscillator 10MHz at 5.10 -7
- Register for Universal Time, Countdown Time
- 2 x **D**irect **D**igital **S**ynthesizer with high resolution, up to 0.5µHz
- Multiple isochronous output clocks with start/stop mode
- Register for Universal Time (TU) and Countdown Time (TD)
- Ability to write directly on the VME the TU and TD
- Differential 7-bit bus for inter-boards synchronization



## Description

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AFAQ ISO 9001 VERSION 2000

# ICV 502

## SPECIFICATIONS (t = 25°C)

| | |
|---|---|
| **TYPE** | SYNCHRONIZED GENERATOR FOR ISOCHRONOUS CLOCK |
| **TIME REGISTERS** | |
| - TUB Register | **T**ime **U**niversal **B**ase: **TUB**<br>32-bit unsigned Binary coded 01.01.1970 origin and the time unit is the second |
| - TUM Register | **T**ime **U**niversal **M**illiseconds: **TUM**<br>32-bit unsigned binary coded. The time unit is the hundred microseconds (high resolution TUB) |
| - TD Register | Time Countdown Register<br>This time is a signed 32-bit number in two complements.<br>Time unit is one millisecond |
| **GPS Module (option)** | |
| - Acquisition of Time ref. | 8 satellites on L1 (1575MHz) as time reference |
| - Frequency and time Distr. | 1pps TTL output<br>10MHz sinewave output<br>Time of Day output |
| - Control | Main status are available via a TTL interface (VME)<br>Time scale UTC or GPS is programmable |
| - Frequency outputs (10MHz) | ≤± 2 x 10 -12 |
| (pps) | ± 50ns |
| - Medium term stability | 3 x 10 -10 / day |
| - Short term stability | 5 x 10 -11 @ 10ms |
| - Cold startup time | ≤ 20mn |
| **CLOCKS OUTPUTS** | |
| - Internal oscillator | 10MHz @ 5 x 10 -7 |
| - Outputs | 1 x pps 1 x 1KHz 1 x 10MHz<br>2 x Direct Digital Synthesizer |
| - DDS Spec. | Primary frequency 128MHz<br>48-bit programmable frequency control<br>Resolution 0,5µHz<br>Parallel Control Interface for fast tuning |
| **LOGIC OUTPUTS** | |
| - Output type | LVDS |
| - Number | 7-bit bus for inter boards synchronization |
| - Others | Gate output and trigger output |
| **VME INTERFACE** | |
| - Transfers | Standard A24 / D16 ; AM 39H, 3DH |
| **POWER SUPPLY** | |
| - Voltage | + 5V / 3A |
| **PRESENTATION** | |
| - Format | VME double EUROPE / 4 Te |
| - Dimensions in mm | 233.35 x 160 |
| - Front panel connectors | 3 "D" 50 pins female connectors |
| **ENVIRONMENT** | |
| - Operating temperature | - 20°C to + 70°C |
| - Storage temperature | - 25°C to + 85°C |
| - Relative humidity | 90 % (without condensation) |
| **EUROPEAN NORMS** | |
| | EMC - EN 61326 - EN 55011 Class A<br>CE Compliance<br>ROHS - 2002/95/EC |

## HOW TO ORDER? ICV 502

## ACCESSORIES

ADAS électronique

*TRACEABILITY FORM*
**DOCUMENT FOLLOW-UP**

***Title:***
*Titre :*

# ICV 502

## English documentation

**Edition: 1** (Document creation - *Création du document*)

| | | | | | |
|---|---|---|---|---|---|
| Written | by | B. THOUËNON | on | 10/10/01 | Visa |
| Revised | by | Ph. DUTIN | on | 10/10/01 | Visa |
| Approved | by | D. PIMONT | on | 10/10/01 | Visa |

**Warning**: Unless otherwise stated, this revision overwrites the previous one, which must be destroyed, along with any copies given to your collaborators.

***Avertissement*** *: En l'absence d'indication contraire, cette nouvelle édition annule et remplace l'édition précédente qui doit être détruite, ainsi que les copies faites à vos collaborateurs.*

| **Edition** *Edition* | **Nature of the modifications (key words)** *Nature des évolutions (mots clés)* | **Written** *Rédigé* | **Revised/Approved** *Revu/Approuvé* |
|---|---|---|---|
| **2** | Annule et remplace édition 1<br>(édition préliminaire)<br>Rev. A | by B. THOUËNON<br>on 22/03<br>Visa | by D. PIMONT<br>on 22/03<br>Visa |
| **3** | Mise à jour de la documentation<br><br>Rev. A | by B. THOUËNON<br>on 22/28<br>Visa | by D. PIMONT<br>on 22/28<br>Visa |
| **4** | Bilingual documentation<br>*Documentation bilingue*<br>Rev. A | by B. THOUËNON<br>on 22/38<br>Visa | by D. PIMONT<br>on 22/38<br>Visa |
| **5** | | by<br>on<br>Visa | by<br>on<br>Visa |
| **6** | | by<br>on<br>Visa | by<br>on<br>Visa |

**DOCUMENT ARCHIVED**
*DOCUMENT ARCHIVE*
No ☐ Yes ☐ on _____

**Δ ed. .. [ ]** = Document input/output *(Entrée/sortie modification de la documentation)*
**# ed. .. [ ]** = Board new function input/output *(Entrée/sortie nouvelle fonctionnalité du produit)*

***NOTES :***

# ICV 502

## SUMMARY

# Chapter A Overview

The **ICV 502** board is a **VME** board for universal time management and for generating synchronous clocks for real-time acquisition systems.

>>>The board features three time management registers:

- Universal Time Base (TUB) register to be initialized to the value of the UNIX date, in the number of seconds since January 1, 1970. This time is a signed 32-bit binary coded number, and the time unit is the second.

- Universal Time register (TUM) containing the number of milliseconds (or hundreds of microseconds, at choice), since the first second after writing to the TUB. This time is an unsigned 32-bit binary coded number, and the time unit is one hundred microseconds.

- Time Countdown register (TD), containing the time remaining before an event (negative value) or the time since an event (positive value). This time is a signed 32-bit number in twos complement, and the time unit is one millisecond.

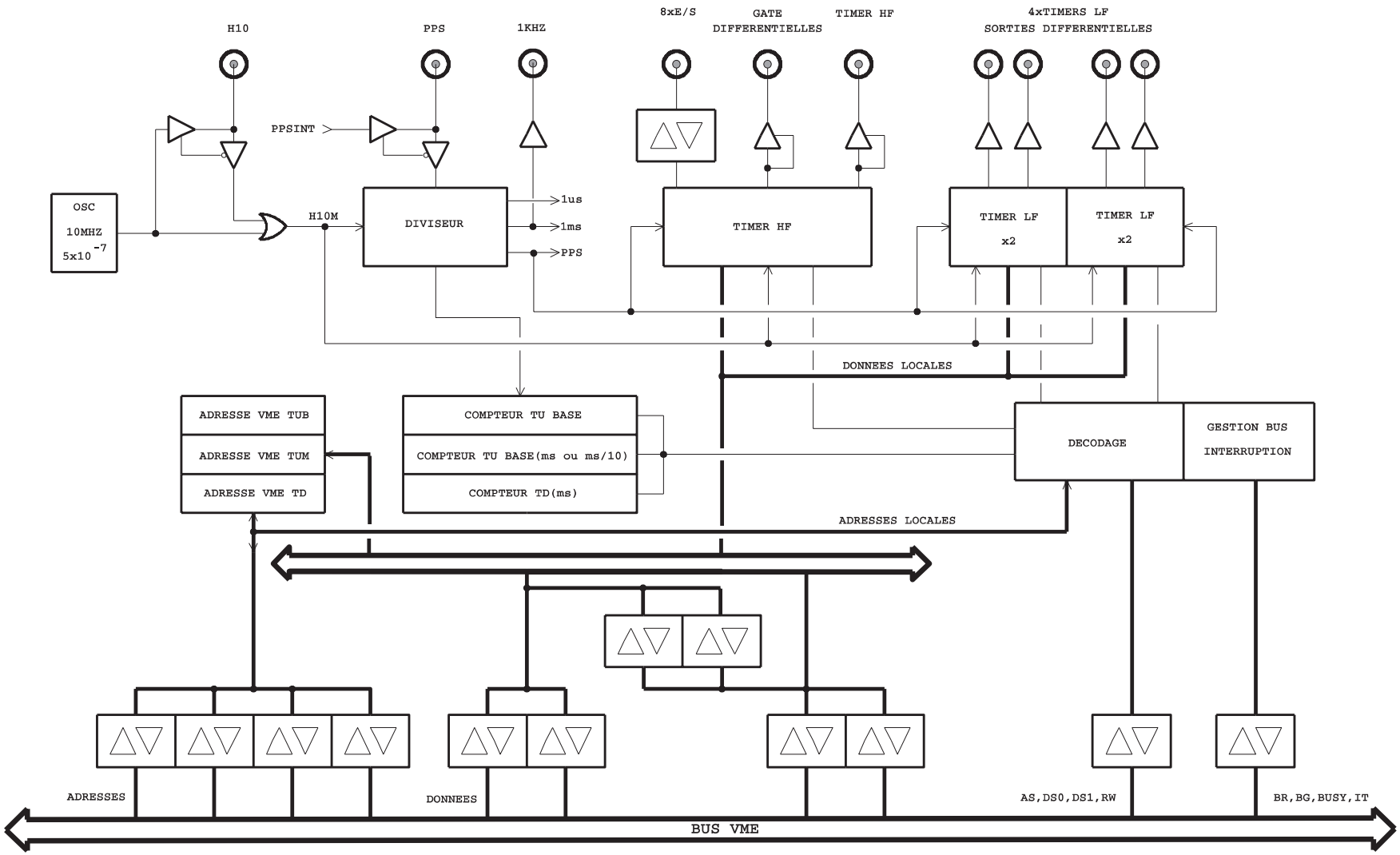
>>>The board generates six clocks in three groups:

- One HIGH FREQUENCY (HF) acquisition clock for analog boards managed by ICV 10Xs.

- Four LOW FREQUENCY (LF) acquisition clocks for autonomous asynchronous boards to be synchronized (ICV 140 LF).

- One 1 KHz clock.

The figure below shows the board's various resources.

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| ADAS électronique | ICV502 | INDICE : A1 \| 15/01/2002 | 1 / 1 |
| | | SYNOPTIQUE | |

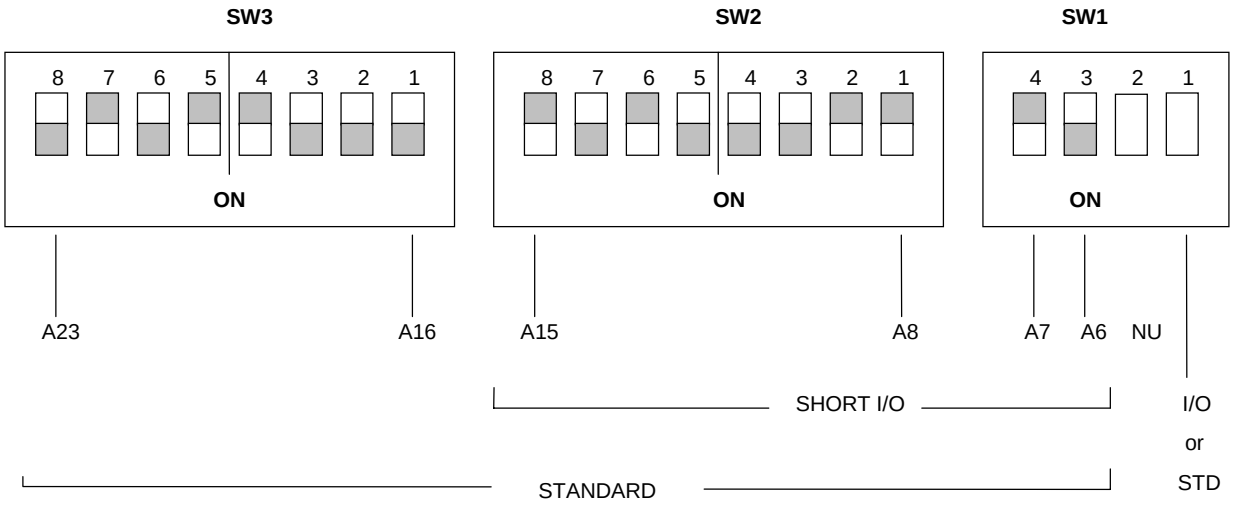
# Chapter B Installation

## Choosing the ICV 502 address seen from the VME bus

The **ICV 502** board occupies 64 bytes in the I/O space or standard space of the **VME** bus.

It can be accessed in 8/16/32 bit mode depending on the registers.

The board's base address is encoded by switches SW3 to SW1.

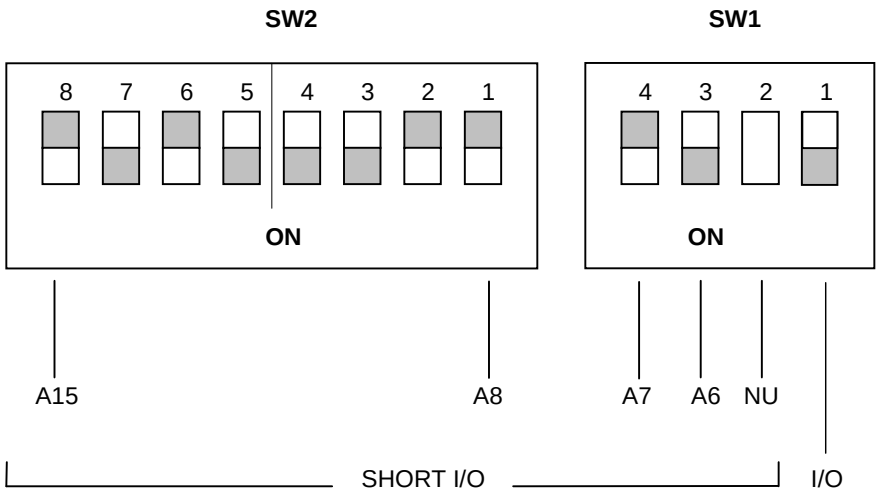



A switch set to "ON" represents a logical "0".
A switch set to "OFF" represents a logical "1".

## Using the I/O space:

Switch SW3 is not significant.
Switch SW1.1 must be set to ON.

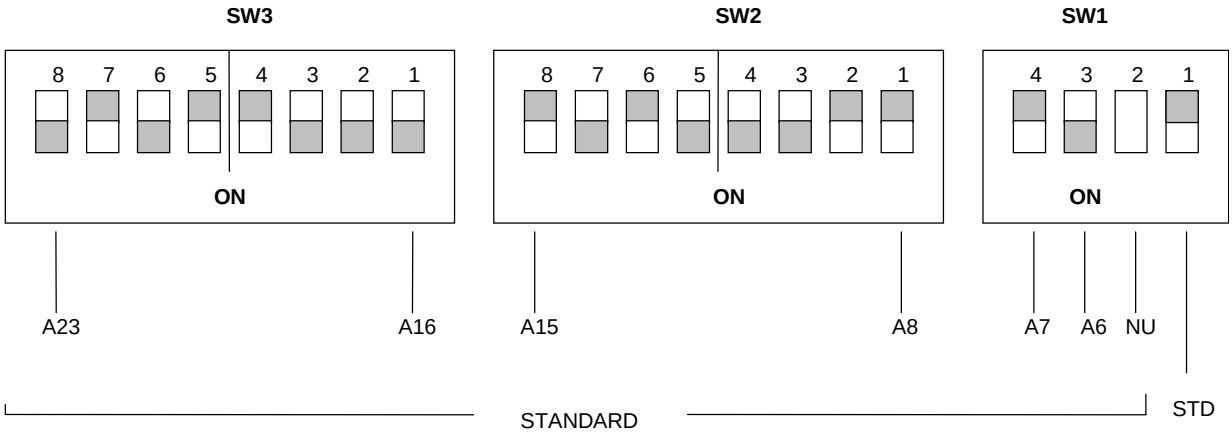
Example: Chosen base I/O address: A380H




## Using the standard space:

Switch SW1.1 must be set to OFF

Example: Chosen standard base address: 58A380H

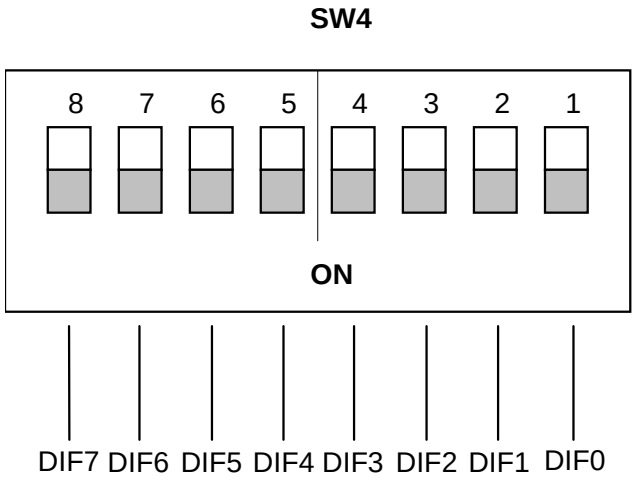


# Switch for closing differential links

The 8 input/output bits of the differential link must be adapted with loop-closing resistances when the board is located at the end of the link. Switch SW4 is provided for that purpose.

Switches that are “ON” represent a closed loop for the 8 bits DIF[7..0].

All 8 switches must be in the same position.



# Chapter C Operations

## C.1. Definition of signals on the front panel

The **ICV 502** board includes several front-panel connectors. This section describes the signals on those connectors.

Δ # ed. 2 [

### C.1.1. The ICV 502 board as an external driver

>>> 10 MHz clock as input

When the board is programmed as an external driver, the 10 MHz reference clock must be provided on LEMO connector J2.

The signal must have a cyclic ratio of 50% +/-5% and must be at TTL levels.

Bit D0 in the control register determines the choice of external or internal clock.

>>> PPS (Pulse Per Second) clock as input

When the board is programmed as an external driver, the PPS (Pulse Per Second) clock must be provided on LEMO connector J3.

The signal must be active high, the width of a “one” pulse must be between 1 µs and 500 ms, and TTL levels must be used.

*Note 1*: Bit D1 in the control register can be used to invert the signal.
*Note 2*: As an external driver, the 10 MHz and PPS clocks cannot be dissociated. in order for the board to operate correctly (e.g. outputs of a GPS board).

Δ # ed. 2 ]

## C.1.2. The ICV 502 board as an internal driver

>>>10 MHz clock as output

When the board is programmed as an internal driver, the 10 MHz reference clock is provided by a local, high-precision, thermostatically controlled oscillator with a frequency stability of **$5.10^{-7}$**. This driver frequency is output on LEMO connector J2.

The signal has a cyclic ratio of 50% and uses TTL levels.

>>> PPS (Pulse Per Second) clock as output

When the board is programmed as an internal driver, the PPS (Pulse Per Second) clock is output on LEMO connector J3.

The signal is generated by the thermostatically controlled oscillator and therefore the frequency stability is identical.

The signal has a cyclic ratio of 50% as uses TTL levels.

## C.1.3. 1 KHz clock

A 1 KHz clock is derived either from the thermostatically controlled local oscillator or from the external driver, as determined by bit D0 in the control register (choice of internal or external clock).

This frequency is output on LEMO connector J1.

The signal has a cyclic ratio of 50% as uses TTL levels.

## C.1.4. Low frequency (LF) clocks

Four clocks generated by timers LF1, LF2, LF3, LF4 are available on LEMO connectors J4, J5, J6, J7, respectively.

These clocks are all isochronous: they can have different frequencies between 500 KHz and 0.15 Hz.

Signals are active low, the width of pulses at zero is 100 ns, and they are issued in differential mode by high-speed line drivers.

## C.1.5. High frequency (HF) clock

One clock provided by the HF timer is available as output on the 25 pin subD connector J8.

This clock is isochronous with the LF clocks as well as with the time registers. Its frequency can vary from 5 MHz to 100 Hz.

The signal has a cyclic ratio of 50% and is issued in differential mode by a high-speed line driver.

This signal is in a stable state (high impedance) at power-on. It is controlled by bit D3 (HM) of the control register.

## C.1.6. GATE Signal

Δ # ed. 3 [

The GATE signal is enabled/disabled by writing to the START/STOP register at base address + 2CH.

This signal is in a stable state (high impedance) at power-on. It is controlled by bit D3 (GATEN) of the control register.

The GATE signal is sent in differential mode by a high-speed line driver on the 25 pin subD connector J8.

Δ # ed. 3 ]

## C.1.7. Eight differential input/output bits

The **ICV 502** board features 8 differential inputs/output to facilitate exchange between the ICV 10X and **ICV 502** boards.

The 8 bits operate in set/reset mode with a general reread of all 8 bits. Only one board can set 1 of the 8 bits as output.

The 8 input/output bits are sent in differential mode by high-speed line drivers on the 25 pin subD connector J8.

Δ # ed. 2 [

# C.2. Mapping

| | | | | | |
|---|---|---|---|---|---|
| 3CH | | Set Reset DIFF 6 | | Set Reset DIFF 7 | R/W |
| 38H | | Set Reset DIFF 4 | | Set Reset DIFF 5 | R/W |
| 34H | | Set Reset DIFF 2 | | Set Reset DIFF 3 | R/W |
| 30H | | Set Reset DIFF 0 | | Set Reset DIFF 1 | R/W |
| 2CH | | Start / Stop | | STATUS DIFF 8 | R/W |
| 28H | | Vector + level Interruption | HF TIMER | | RW |
| 24H | LF3 TIMER | | LF4 TIMER | | RW |
| 20H | LF1 TIMER | | LF2 TIMER | | RW |
| 1CH | RAZ TU | | CLEAR TD | | W0 |
| 18H | TD REGISTER | | | | RW |
| 14H | TUM REGISTER | | | | R0 |
| 10H | TU BASE REGISTER | | | | RW |
| CH | TD VME (ms) ADDRESS | | | | R/W |
| 8H | A32 TU VME (ms) ADDRESS | | | | R/W |
| 4H | TU BASE VME A32 (s) ADDRESS | | | | R/W |
| 0H | R 502A / W INIT | | CONTROL REGISTER | | R/W |
| | D31 | | D16 D15 | | D0 |

Δ # ed. 2 ]

# C.3. Definition of registers

## C.3.1. ICV 502 Identification & initialization register

Base address **+ 0H**
This 16-bit register is accessible in read/write mode from the **VME** bus.

In read mode:

A 16-bit access to the base address **+0H** allows to identify the **ICV 502** board. The value read is 502A, representing the **ICV 502** board revision A.

In write mode:

A write access to the base address **+0H** initializes the **ICV 502** board. This write access is dummy (only the address is used).

Δ # ed. 2 [

## C.3.2. Control Register

Base address **+ 2H.** 16-bit read/write access
(MST status 0000H)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PR H10 | PR PPS | | | | ENIT | CH LF34 | CH LF12 | Resol | AV 24 | MTR 1 | MTR 0 | HM | GATE EN | INV PPS | EXT |

**BIT D0** : EXT Choice of reference clock

= 1 The 10 MHz $10^{-7}$ internal oscillator is the reference

= 0 The external (10 MHz) signal input on the LEMO connector
J2 is the reference for the **ICV 502**.

The PPS connector becomes an input.
The MST status is an input

**BIT D1** : INV PPS Choose whether or not to invert the PPS (Pulse Per Second) signal when the external PPS input for on LEMO connector J8 is used.

= 0 Direct input

= 1 Inverted input

**BIT D2** : GATE EN This bit enables the GATE as an output on the 25 pin subD connector J8.
The GATE in output mode allows you to start acquisition on the slave coupling boards
(Clock and Gate in Flip-Flop mode on the ICV 107)

= 0 GATE output is stable (high impedance)

= 1 GATE output active; its status depends on the start related to the HF clock.

Δ # ed. 2 ]

**BIT D3** : HM This bit enables the HF clock on the25 pin subD connector J8.
The **ICV 502** becomes the master board (Master Clock)

= 0 The **ICV 502** does not output the HF clock on the J8 connector

= 1 The **ICV 502** outputs the HF clock on the J8 connector (it is used to synchronize the acquisition on ICV 107 slave boards).

**BIT D4** : MTR0 Code for choosing the write frequency on the **VME**
**BIT D5** MTR1 bus of the TU Base, TU ms, TD registers

| MTR1 | MTR0 | |
|---|---|---|
| 0 | 0 | No VME access |
| 0 | 1 | Request access every 100µs |
| 1 | 0 | Request access every 1 ms |
| 1 | 1 | Request access every 10 ms |

**BIT D6** : AV24 Choose the space used by the **ICV 502** board when it writes to the **VME** the values of the TUB, TU and TD registers.

= 0 The extended space (A32) is used

= 1 The standard space (A24) is used. In this case bits A31 $\Rightarrow$ A24 in the TUB, TU, and TD address registers are not significant.

**BIT D7** : Resol Chooses the resolution of the Universal Time counter TU

= 0 The increment value is one millisecond

= 1 The increment value is 1/10 millisecond (100µs)

When a one ms resolution is used, the duration of the TU counter is on the order of 50 days (for the higher resolution, the duration is reduced to 5 days).

Δ # ed. 3 [

**BITS D8, BIT D9** Choose the resolution of the LF timer clocks.
Bit D8 : CHLF12 used for clocks LF1 and LF2
Bit D9 : CHLF34 used for clocks LF3 and LF4
When bits D8 and/or D9 are set to 0, the basic clocks of the corresponding LF timers are set to 1 MHz.
When bits D8 and/or D9 are set to 1, the basic clocks of the corresponding LF timers are set to 10 KHz

Δ # ed. 3 ]

**BIT D10** : ENIT Used to authorise/prevent the generation of an interruption on the **VME** bus when the **ICV 502** board writes the TU Base, TU and TD registers on the **VME**.
Therefore this interruption is recurrent at the same frequency as writes registers on the **VME** bus. (choice of 100µs, 1ms, or 10ms)

= 0 Interruption disabled

= 1 Interruption enabled

Δ # ed. 2 [

**BITS D11, D12, D13** Reserved bits

Δ # ed. 2 ]

**BIT D14** : PR PPS Read-only bit. Indicates that the pulse per second is present if its value alternates between 1 and 0.
If the value remains at “0”, there is no input signal.

**BIT D15** : PR H10 Read-only bit. Indicates the presence of the 10 MHz clock in input on the LEMO connector J2 if D15 equals “1”.
D15 at “0” indicates there is not input signal.

## C.3.3. VME address registers

**VME** address register TU Base (basic universal time)
**VME** address register TU (universal time)
**VME** address register TD (Countdown time)

The values of these registers can be written to the addresses defined in the 3 **VME** address registers.

**VME address register TU Base**: 32 bit read/write access
Base address **+ 04H**

This 32 bit register contains the address where the **ICV 502** board will read the value of the TU Base register

| D31 | D24 | D23 | D16 | D15 | D8 | D7 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| A31 | A24 | A23 | A16 | A15 | A8 | A7 | A2 | 0 | 0 |

Δ # ed. 2 [

Addresses A0 and A1 are forced to “0”, as the word to be transferred includes 32 data bits.

Addresses A31 to A24 are not significant when bit D6 in the control register AV24 = 1 (standard address space)

**VME address register VME TU**: 32 bit read/write access
Base address **+ 08H**

**VME address register VME TD**: 32 bit read/write access
Base address **+ 0CH**

*Both these registers are identical to the TU Base register*

Δ # ed. 2 ]

Δ # ed. 2 [

## C.3.4. Time registers

TU Base (basic universal time) register
TU (universal time) register
TD (countdown time) register

**TU Base Register**: 32 bit read/write access
Base address **+ 10H** MST status 0000.0000.H

This register, which manages universal time, will be initialized via the **VME** to the UNIX date: number of seconds (unsigned integer) since January 1, 1970.

**TU Register**: 32 bit read-only access
Base address **+ 14H** MST status 0000.0000.H

This register, with an unsigned binary coded, is incremented either each millisecond or each 1/10 millisecond (determined by bit D7 ‘’Resol’’ in the control register)

The register can count to approx. 50 days (ms) or 5 days (1/10 ms)

**It is incremented at the first PPS following a write to TUB**

Time is managed even when the Reset TU command is issued or when the TU counter overflows. **The TU Base is incremented automatically and the TU is reset to 0.**

**TD Register**: 32 bit read/write access
Base address **+ 18H** MST status 8000.0000.H

This register contains a signed 32-bit number in twos complement which may be preloaded. The counter is incremented every millisecond.

The time counted can range from –25 days to +25 days.

This register supports the START, STOP, and CLEAR modes.

Δ # ed. 2 ]

### C.3.5. Reset TU command

16 bit write-only access

A dummy write to the base address **+ 1CH** resets the TU register to zero, and the TU Base register is incremented by the number of seconds contained in TU.

Δ # ed. 2 [

### C.3.6. Clear TD command

16 bit write-only access

A dummy write to the base address **+ 1EH** resets the TD register to 8000.0000.H.

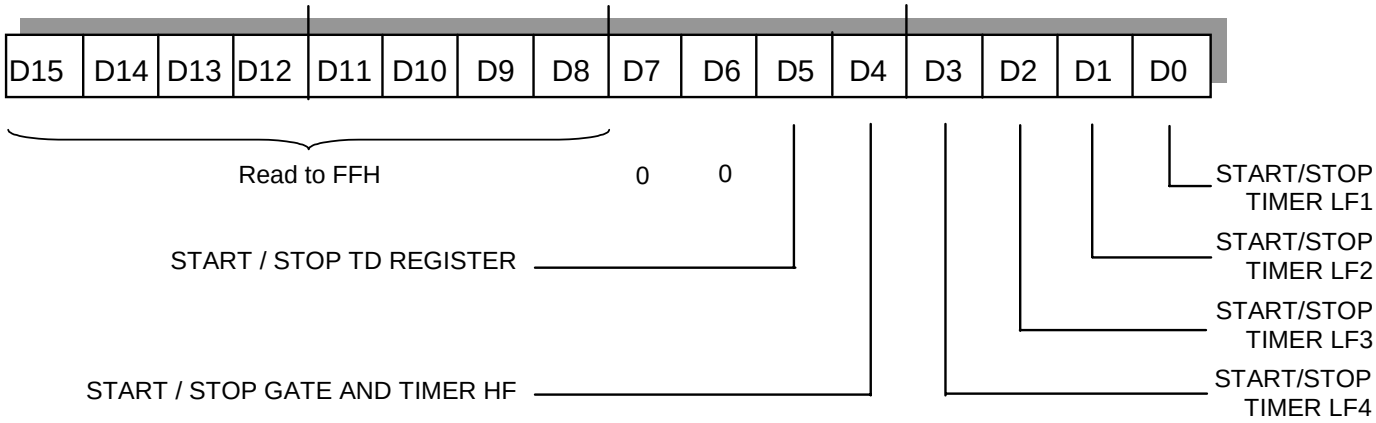
*>>>Note:*
The counter resumes counting if the STOP command did not precede the CLEAR command.

Δ # ed. 2 ]

∆ # ed. 2 & 3 [

## C.3.7. START/STOP command

16 bit read/write access
Base address **+ 2H**




The START/STOP command works by bit. You can start the timers and the gate individually or simultaneously.

A write operation with one or more bits set to “1” will START the concerned functions.
A write operation with one or more bits set to “0” will STOP the concerned functions.

The START / STOP commands for the LF1 to LF4 timers and the general GATE are synchronised on the start of the PPS second.

The START is saved, and the next Pulse Per Second (PPS) starts the timers and/or the GATE.

The STOP is saved, and the next Pulse Per Second (PPS) stops the timers and/or the GATE.

∆ # ed. 2 & 3 ]

Δ # ed. 2 [

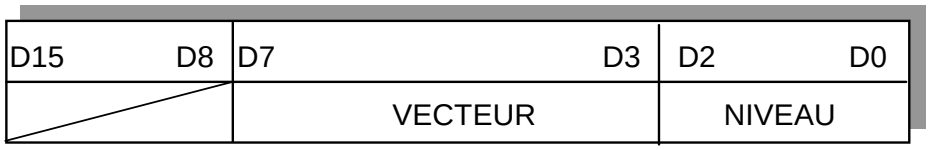
## C.3.8. Interrupt vector and level

16 bit read/write access
Base address **+ 28H**

The **ICV 502** board can generate periodic interrupts if bit D10 (ENIT) in the control register is set to “1”.

The interrupt period depends on the period of writes the TUB, TU and TD registers on the **VME** bus.

An interrupt is issued after writing three 32-bit words. The interrupt vector and level are defined in this register.




The vector is defined by the 5 bits D7 – D3.

Bits D2 to D0 are forced to “0”.

The interrupt level is defined by bits D2, D1, and D0 according to the following binary code:

| | D2 | D1 | D0 |
|---|---|---|---|
| IT7 level | 1 | 1 | 1 |
| IT6 level | 1 | 1 | 0 |
| IT5 level | 1 | 0 | 1 |
| IT4 level | 1 | 0 | 0 |
| IT3 level | 0 | 1 | 1 |
| IT2 level | 0 | 1 | 0 |
| IT1 level | 0 | 0 | 1 |
| No IT | 0 | 0 | 0 |

Δ # ed. 2 ]

Δ # ed. 2 [

## C.3.9. SET/RESET 8 differential input/output bits

The board can generate and receive 8 bits on the front panel. These bits are handled individually (in set/reset mode) and can be read by byte.

Each bit is sent to and received from the front panel in differential mode.

Each bit is sent in self-enabled mode (that is, if a bit is not set, it will remain in a stable state); it is thus possible to create an 8-bit bus.

*Note*:
A bit can be set by only one ICV10X or **ICV502** board.

Each bit is controlled by its own address
(base register **+ 30H** to base **+ 3EH**).

The D0 bit of each address is used to set or to disable the output bit.

A write to the output bit address with D0 set to "0" will set that bit to zero.

A write to the output bit address with D0 set to "1" will reset that bit (stable state).

The status of the 8 bits can be read at the same address (MST Status FFH).

Only the status of the 8 bits on the board is read, and not the status of the bits set on the front panel connector.

Δ # ed. 2 ]

Δ # ed. 2 & 3 [

## C.3.10. Reading the byte for differential inputs

The status of the bits on the connector can be read in the base register **+2EH**.

Bit D7 represents the status of differential input 7
Bit D6 represents the status of differential input 6
Bit D5 represents the status of differential input 5
Bit D4 represents the status of differential input 4
Bit D3 represents the status of differential input 3
Bit D2 represents the status of differential input 2
Bit D1 represents the status of differential input 1
Bit D0 represents the status of differential input 0

A bit set to “1” indicates high impedance (stable), and “0” indicates an active bit.

Δ # ed. 2 ]

## C.3.11. Acquisition frequency register – HF Timer

This register contains the value of the HF acquisition frequency.
This signal is used to synchronize the acquisition of ICV 10X boards. It will be issued on the J8 connector after validating the D2 (GATEN) and D3 (HM) bits in the control register and the D4 general start bit of the START/STOP register.

16-bit read/write access, base address + **2AH**

This 16-bit timer has a resolution of 200ns (5 MHz).

The frequency value equals

$$F = \frac{5MHz}{n+1} \quad 0 \le n \le 2^{16} - 1$$

Frequency between 5 MHz and approx. 100 Hz

Example: Acquisition at 200 KHz ==> n = 24

Δ # ed. 3 ]

## C.3.12. Acquisition frequency register – LF Timers

The **ICV 502** features 4 LF registers. These four registers are designed to manage low frequencies during acquisition on ICV 10X boards.

The four frequencies are isochronous and may be triggered simultaneously by the START/STOP register.

16 bit read/write access

| | |
|---|---|
| Fréquence LF1 | Adresse base + **20H** |
| Fréquence LF2 | Adresse base + **22H** |
| Fréquence LF3 | Adresse base + **24H** |
| Fréquence LF4 | Adresse base + **26H** |

For these 16-bit timers, you can choose a resolution of 1 µs (1 MHz ) or 100 µs (10 KHz).

The frequency value equals

$$F = \frac{1MHz}{n+1} 1 \le n \le 2^{16} - 1$$

Frequency between 500 KHz and approx. 15 Hz

Example: Acquisition at 2000 Hz ==> n = 499

$$F = \frac{10KHz}{n+1} 1 \le n \le 2^{16} - 1$$

Frequency between 5 KHz and approx. 0.15 Hz

Example: Acquisition at 1 Hz ==> n = 9999

# Chapter D Master mode

The **ICV 502** board can write the values of the TUB, TU, and TD registers, representing three 32-bit words at the three addresses defined in the following registers:

- **VME** TUB address base + 04H,
- **VME** TU address base + 08H,
- **VME** TD address base + 0CH.

The three words may be written in extended or standard mode, as determined by bit D6 (AV24) in the control register.
The chosen mode applies to all three words.

Access requests to the **VME** bus are defined by the MTR0 and MTR1 bits in the control register at the base address + 2H.

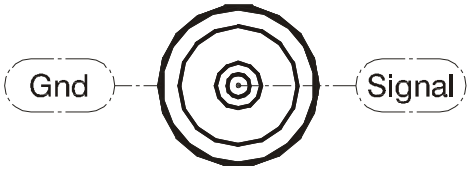
During these accesses, the VGT (Vme GranT) LED turns on.

# Chapter E Connections

## E.1. J1 connector

LEMO J1

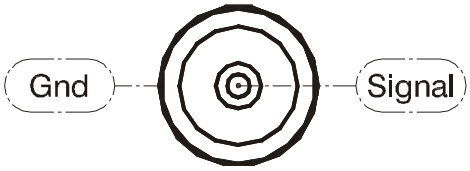
Timer 1KHz



## E.2. J2 connector

LEMO J2

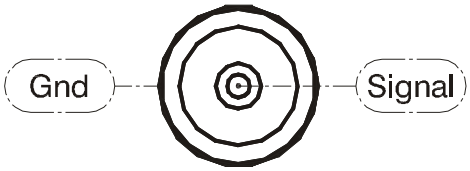
Timer 10 MHz



## E.3. J3 connector

LEMO J3

PPS (Pulse Per Second)



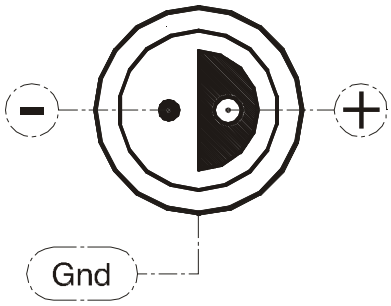
## E.4. J4 to J7 connectors

LEMO J4 to J7

**HEX +**

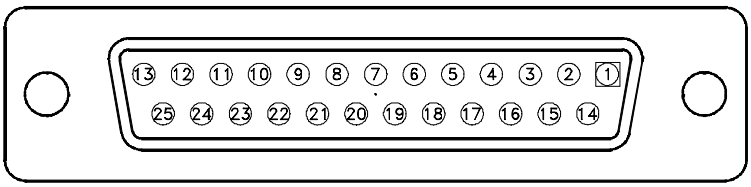
**HEX -**

Differential output of the LF clock



# E.5. J8 connector

## DB 25S




| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| **1** | DIF0 + | | |
| | | **14** | DIF0 - |
| **2** | DIF1 + | | |
| | | **15** | DIF1 - |
| **3** | DIF2 + | | |
| | | **16** | DIF2 - |
| **4** | DIF3 + | | |
| | | **17** | DIF3 - |
| **5** | DIF4 + | | |
| | | **18** | DIF4 - |
| **6** | DIF5 + | | |
| | | **19** | DIF5 - |
| **7** | DIF6 + | | |
| | | **20** | DIF6 - |
| **8** | DIF7 + | | |
| | | **21** | DIF7 - |
| **9** | NC | | |
| | | **22** | GATE - |
| **10** | GATE + | | |
| | | **23** | NC |
| **11** | NC | | |
| | | **24** | GND |
| **12** | HEX+ | | |
| | | **25** | HEX - |
| **13** | GND | | |

**DIF[7..0] +**
**DIF[7..0] -** } 8 differential Inputs/Outputs linked to registers 30H to 3EH

**GATE +**
**GATE -** } Differential output START of acquisition

**HEX +**
**HEX -** } Differential output of the HF clock > ICV10X

**GND** : Logical ground

# Chapter F Visualization

The **ICV 502** board includes two LEDS:

**ACC LED** : This LED (ACCess) indicates an access from the **VME** bus in slave mode.

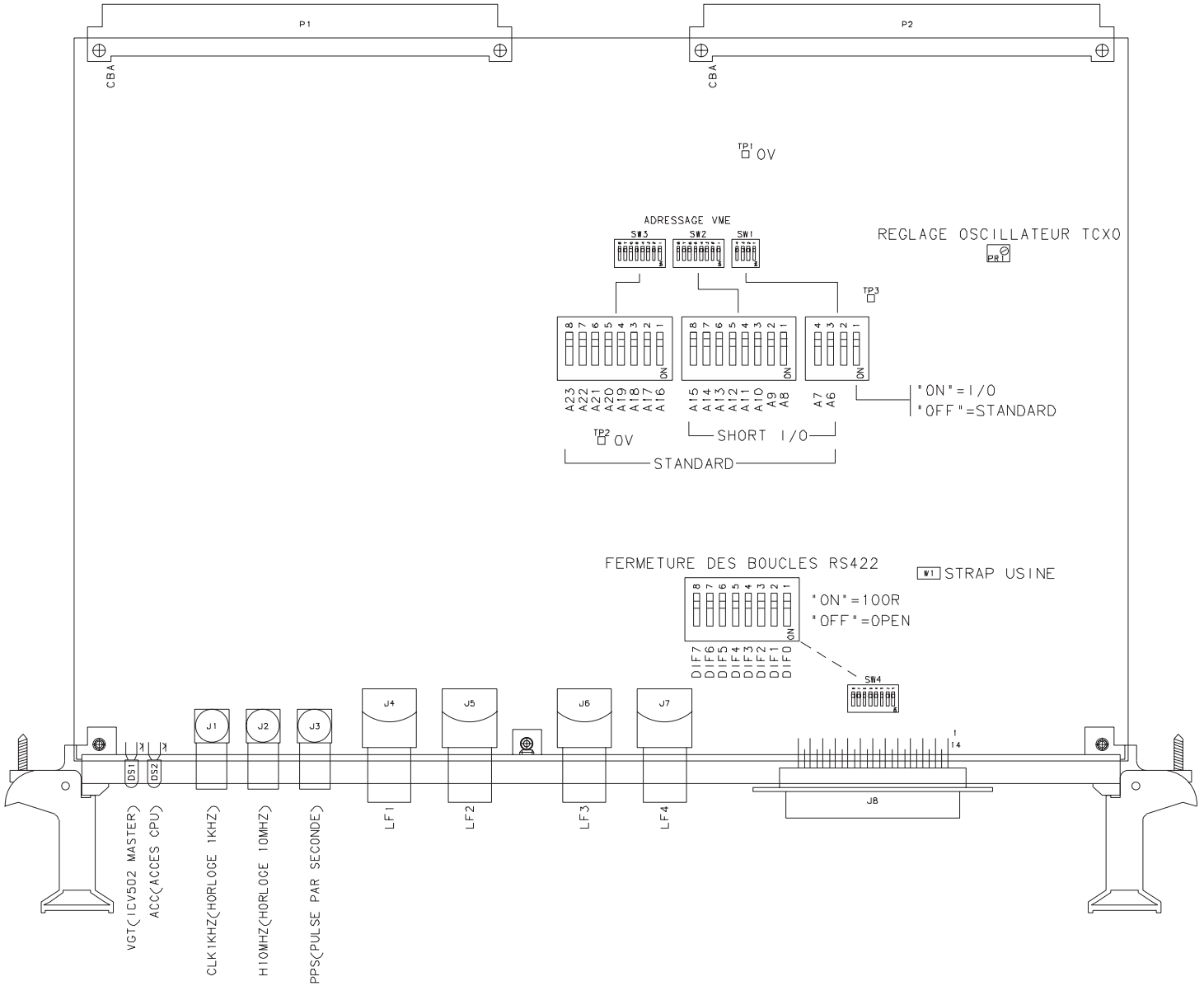
**VGT LED** : This LED (Vme GranT) indicates an access by the **ICV 502** to the **VME** bus in master mode.

# Appendix

## CONFIGURATION LAYOUT

## EQUIPMENT LAYOUT

## FRONT PANEL LAYOUT




INDICE DE REVISION: A.0

REAL/REV: _____ LE: _____ VISA: _____

APPROUVE: _____ LE: _____ VISA: _____

CREATION DU DOCUMENT: A.0

REAL/REV: MAO LE: 23/10/2001

Ech: 1

PLAN: 1/1

ZAC - 9, rue Georges Besse
78330 FONTENAY LE FLEURY - FRANCE
Tel:(33) 1 30 58 90 09 - Fax:(33) 1 30 58 21 33
e-mail:infoadas@adas.fr - http://www.adas.fr

ADAS électronique

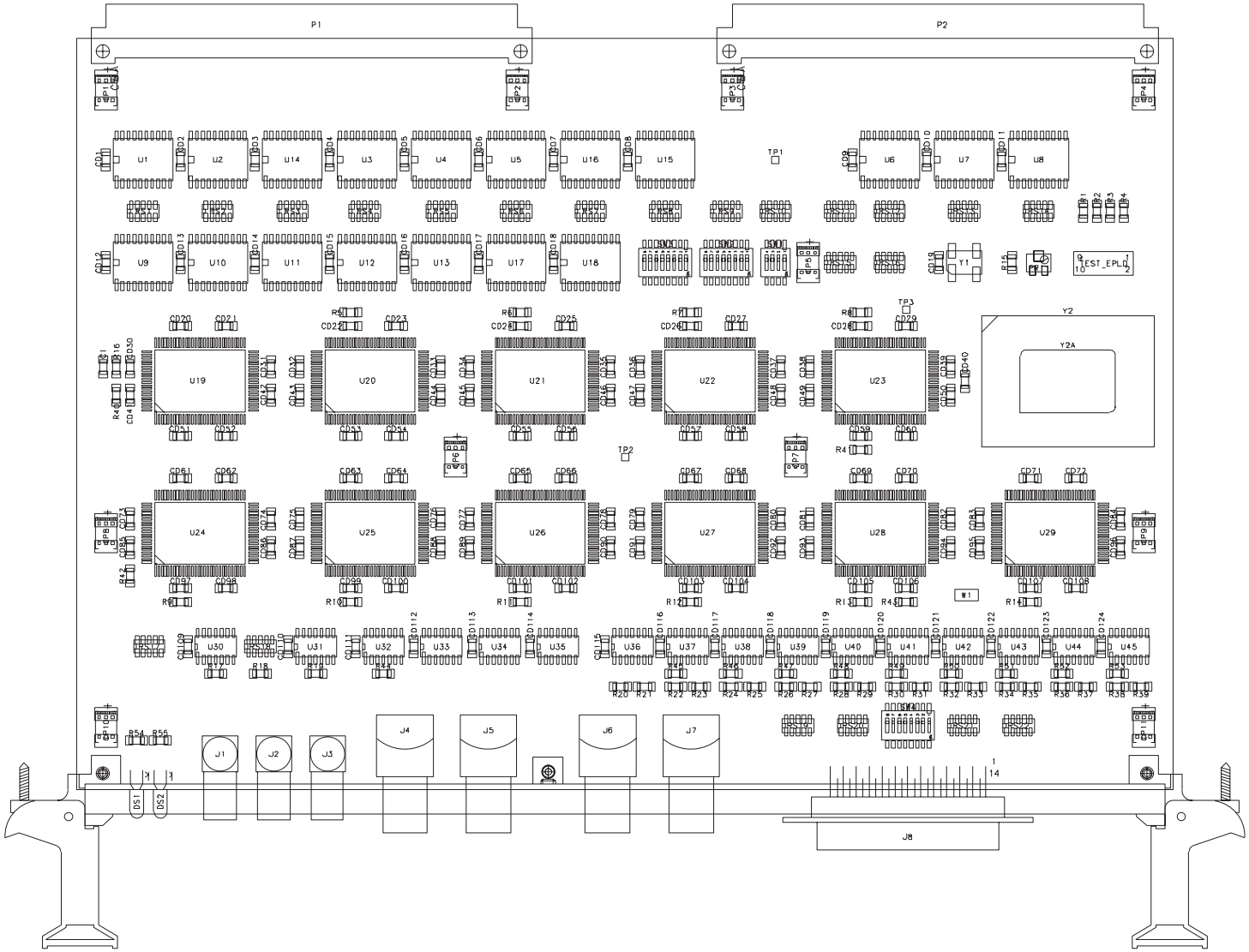
CLIENT: ADAS
REF: XXXXXXXX

FAMILLE: VME

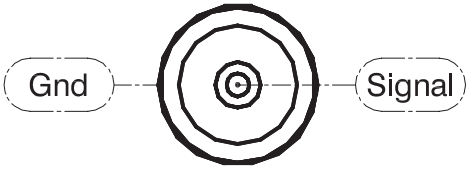
# PLAN DE CONFIGURATION
# COTE SUPERIEUR CARTE

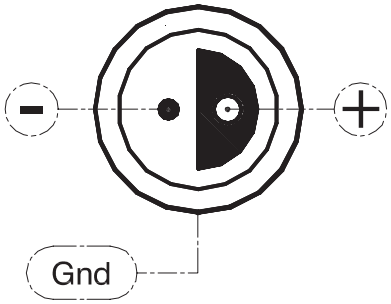
NOM:

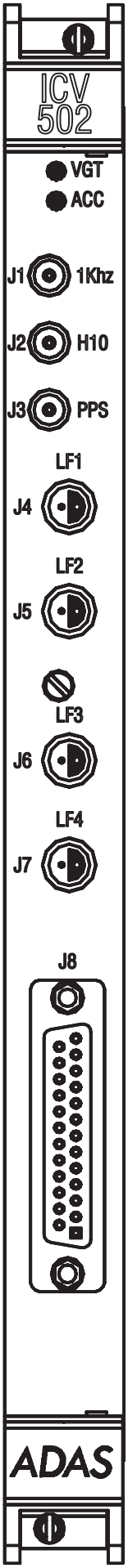
# ICV 502




| | | | |
|---|---|---|---|
| INDICE DE REVISION: A,0 | Ech: 1 | ZAC - 9, rue Georges Besse<br>78330 FONTENAY LE FLEURY - FRANCE<br>Tel:(33) 1 30 58 90 09 - Fax:(33) 1 30 58 21 33<br>e-mail:infoadas@adas.fr - http://www.adas.fr | ADAS électronique |
| REAL/REV: _____ LE: _____ VISA: _____ | | | |
| APPROUVE: _____ LE: _____ VISA: _____ | PLAN: 1/1 | CLIENT: ADAS<br>REF: XXXXXXXX | FAMILLE: VME |
| CREATION DU DOCUMENT: A,0 | PLAN D'EQUIPEMENT<br>COTE SUPERIEUR CARTE | | NOM: ICV 502 |
| REAL/REV: MAO LE: 23/10/2001 | | | |

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| INDICE DE REVISION: A0<br>REAL/REVU : SITH LE: 23/10/2001 VISA:<br>APPROUVE : LE: VISA: | Ech: 1<br>PLAN: 1/1 | ZAC – 9, rue Georges Besse<br>78330 FONTENAY LE FLEURY–FRANCE<br>Tel:(33) 1.30.58.90.09 – Fax:(33) 1.30.58.21.33<br>e–mail: infoadas@adas.fr – http://www.adas.fr<br>CLIENT: ADAS<br>REF: ICV 502 | FAMILLE: MECA |
| CREATION DU DOCUMENT: A0<br>REAL/REVU : SITH LE: 23/10/2001 | FACE AVANT 6U 4TE<br>ICV 502 | | NUMERO :<br>13.2.40.A0–C |