CPCI SYN

SYNCHRONIZATION BOARD BETWEEN RACK

This board has been developed for application where several PXIs rack have to be synchronized.

It provides the emission/reception of gating pulses in real time environments.

Status LEDs allow to visualize the general functioning of the system.

- **2 inputs GATIN PULSE RS485**
- **2 RS 485 sync. tick inputs**
- **2 outputs GATIN PULSE RS485**
- **Emission/Reception of PXI trigger on connector P2**
- **Board status provided by LEDs**

SPECIFICATIONS*

ENVIRONMENT	
Operating temperature	- 20°C to + 70°C
Storage temperature	- 25°C to + 85°C
Relative humidity	90 % non condensing
EUROPEAN STANDARD	
	CE Compliance (EMC - EN 61326 - EN 55011 Class A) ROHS - 2002/95/EC

**Specifications given for 25°C*

ORDERING INFORMATION

CPCI SYN	Synchronization board between rack

APPLICATIONS

ADAS™

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ADAS électronique

TRACEABILITY FORM
DOCUMENT FOLLOW-UP

Title :
Titre :

CPCI SYN

English documentation

Edition : 1 (Document creation - *Création du document*)

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Revised by	D. PIMONT	on	27/17	Visa
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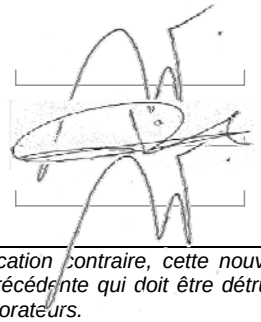

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Edition *Edition*	**Nature of the modifications (key words)** *Nature des évolutions (mots clés)*	**Written** *Rédigé*	**Revised/Approved** *Revu/Approuvé*
2		by on Visa	by on Visa
3		by on Visa	by on Visa
4		by on Visa	by on Visa
5		by on Visa	by on Visa
6		by on Visa	by on Visa

DOCUMENT ARCHIVED
DOCUMENT ARCHIVE
No ☐ Yes ☐ on _____

Δ ed. .. [ ] = Document input/output *(Entrée/sortie modification de la documentation)*
 # ed. .. [ ] = Board new function input/output *(Entrée/sortie nouvelle fonctionnalité du produit)*

NOTES :

SUMMARY

Chapter A Presentation

The **CPCI SYN** board is a Compact Pci board for cross-rack synchronization.

It contains:

- 2 RS 485 sync. tick inputs and 2 RS 485 sync. tick outputs
- one trigger interface (for triggers received/sent) – PXI on P2
- status LEDs

Designed for applications with multiple **CPCI** racks, this board will be used to receive and send sync. signals in real-time environments.

Status LEDs indicate the general performance of the system.

A.1. Wiring and interconnection

If the reader wishes it, application examples of interconnections are given in the chapter Other Services "Wiring and Config" on our Web site.

Chapter B Operation

The **CPCI SYN** board will be used to send and receive sync. signals for multi-rack applications.

Several operating modes are available.

The sync. signals are received on front panel **J1** and **J2** connectors, and are redirected to **J3** and **J4** connectors and backplane PXI triggers.

Backplane **PXI** triggers are bidirectional, which means that the sync. signals can either be sent from a board within the rack that generates the sync. signals (input triggers), or be sent through the backplane to the boards that need to be synchronized (output triggers).

The **CPCI SYN** board has several switches for configuring input & output triggers and operating modes.

Chapter C Configuration Switches

C.1. S1 Switches

S1 switches are used to select which signals will be sent **to** backplane PXI triggers.

SWT 01 (1) and SWT 02 (2) are for PXI trigger 0

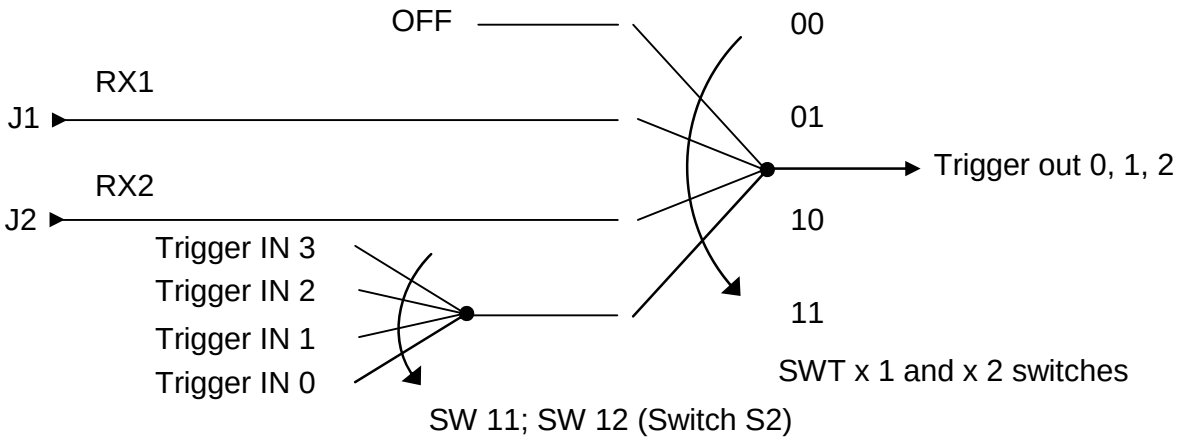
SWT 11 (3) and SWT 12 (4) are for PXI trigger 1

SWT 21 (5) and SWT 22 (6) are for PXI trigger 2

Signal sent to PXI output triggers

SWT x 2	SWT x 1	TRIGGER OUT
OFF	OFF	Disabled
OFF	ON	RX1 signal from J1
ON	OFF	RX2 signal from J2
ON	ON	Trigger IN

PXI TRIGGER OUT BLOCK DIAGRAM



Note: One input trigger cannot be redirected to the same trigger's output.

C.2. S2 switches

S2 switches (1 - 4) let you select which backplane **PXI** input triggers will be redirected to **J3** and/or **J4** outputs.

- S01(1) and S02(2) select which backplane **PXI** input trigger will be redirected to **J3** connector.

J3 OUTPUT

S02(2)	S01(1)	
OFF	OFF	TRIGGER PXI IN 0
OFF	ON	TRIGGER PXI IN 1
ON	OFF	TRIGGER PXI IN 2
ON	ON	TRIGGER PXI IN STAR

Note: One signal sent to **J1** input connector disables **PXI** input triggers; the signal is redirected from **J1** to **J3** connector.

- S11(3) and S12(4) select which backplane **PXI** input trigger will be redirected to **J4** connector

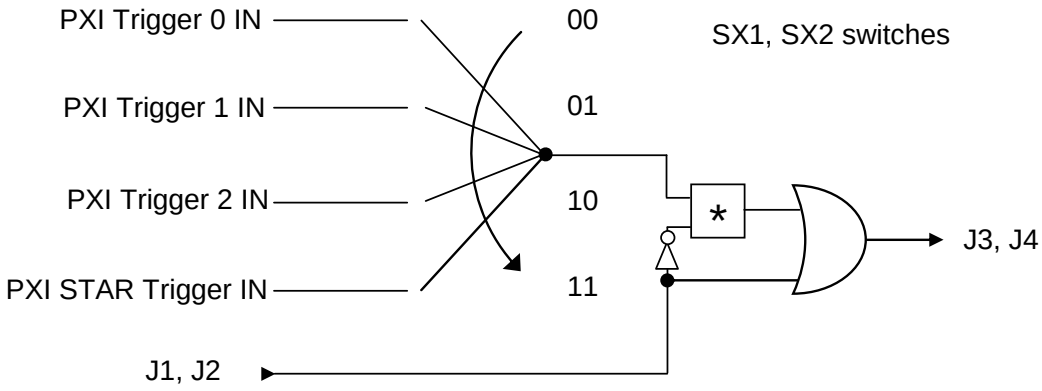
J4 OUTPUT

S12(4)	S11(3)	
OFF	OFF	TRIGGER PXI IN 0
OFF	ON	TRIGGER PXI IN 1
ON	OFF	TRIGGER PXI IN 2
ON	ON	TRIGGER PXI IN STAR

Note: One signal sent to **J2** input connector disables **PXI** input triggers; the signal is redirected from **J2** to **J4**

(provided SW5 et SW6 are not OFF)

PXI TRIGGER IN BLOCK DIAGRAM



Switches SW5 (R012) and SW6 (R034) are used to redirect **J1** and **J2** input signals to J3 and J4.

SW5	**SW6**	
ON	ON	J1 -> J3 J2 -> J4
OFF	ON	J2 -> J3 & J4
ON	OFF	J1 -> J3 & J4
OFF	OFF	J1 & J2 OFF -> J3 & J4

Chapter D Signalling

Each front panel connector is coupled to 3 LEDs:

- 1 green : S
- 1 yellow : R
- 1 red: D

Green LEDs (Signal) are on when a signal is sent to **J1** or **J2** and redirected to **J3** or **J4**.

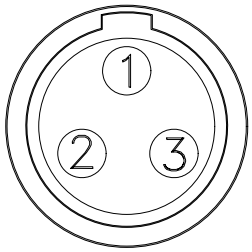
Yellow LEDs (Redundant) are on when using SW5 and SW6 to send *redundant* signals from **J1**, **J2** to **J3**, **J4**.

Red LEDs (Fault) are on when you plug a cable into **J1** or **J2** and no signal is present.

Chapter E Connectors

E.1. J1; J2

RS 485 differential inputs

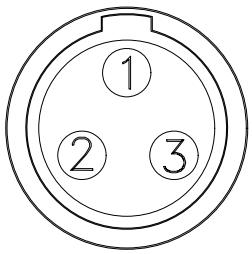


FRONT VIEW

PIN	SIGNAL
1	+ IN
2	- IN
3	Cable IN sensing

E.2. J3 ; J4

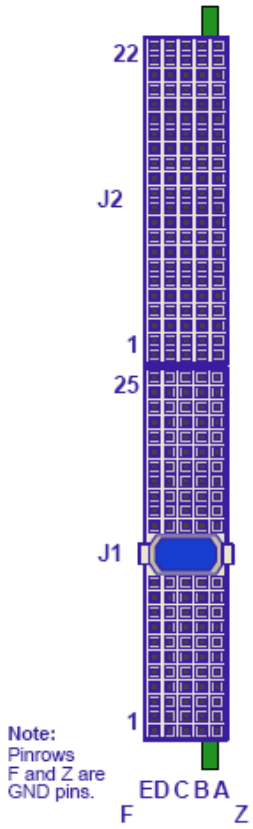
RS 485 differential outputs



FRONT VIEW

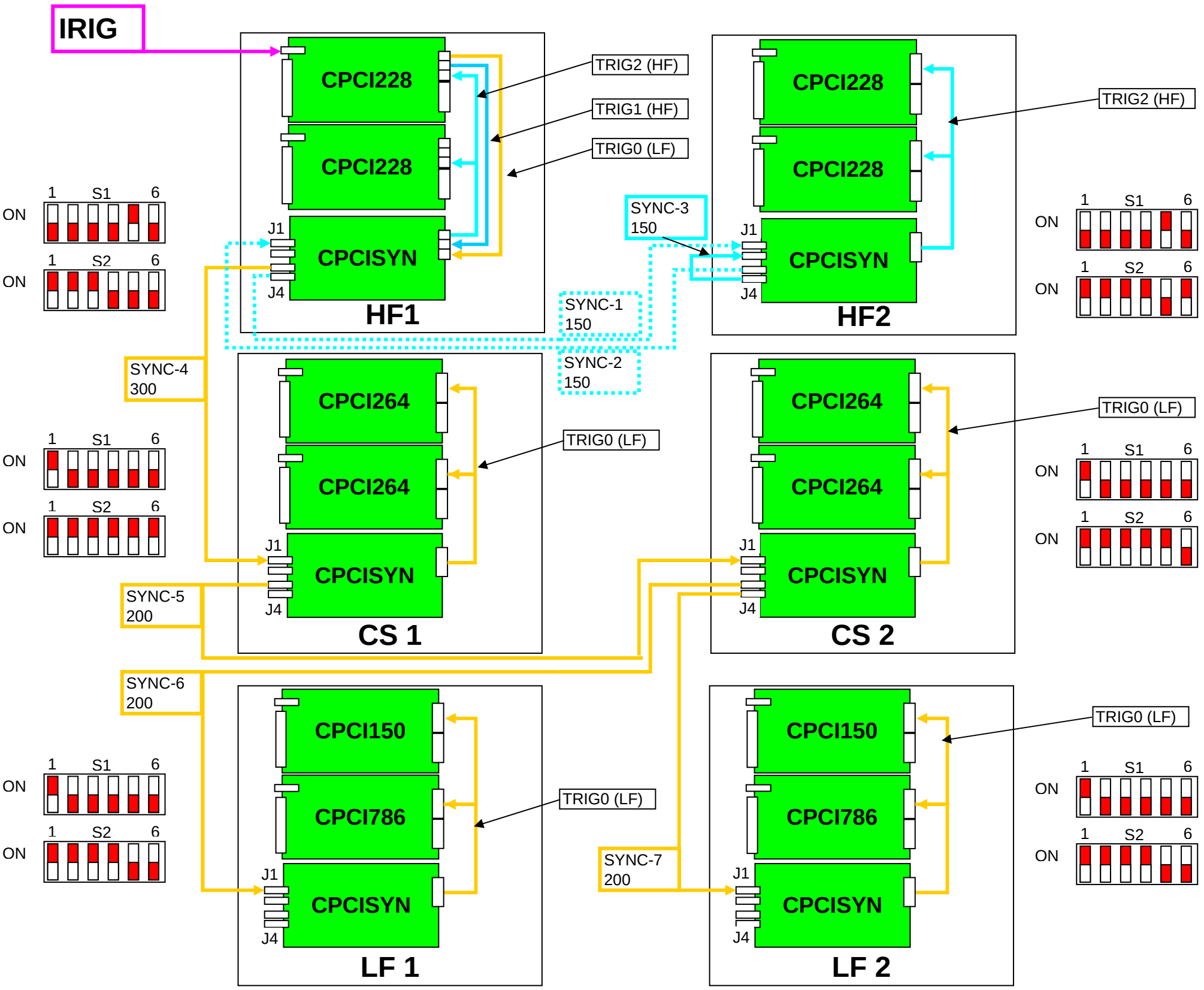
PIN	SIGNAL
1	+ OUT
2	- OUT
3	Cable OUT sensing

E.3. CPCI J2 Pins Used



CPCI J2 PIN ASSIGNMENT
Female connector
Used pins in **bold**

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	NC	PXI_RSVA22	PXI_RSVB22	PXI_RSVC22	PXI_RSVD22	PXI_RSVE22	**GND**
21	NC	**PXI_LBR0**	**GND**	**PXI_LBR1**	**PXI_LBR2**	**PXI_LBR3**	**GND**
20	NC	**PXI_LBR4**	**PXI_LBR5**	**PXI_LBL0**	**GND**	**PXI_LBL1**	**GND**
19	NC	**PXI_LBL2**	**GND**	**PXI_LBL3**	**PXI_LBL4**	**PXI_LBL5**	**GND**
18	NC	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	**GND**	PXI_TRIG6	**GND**
17	NC	**PXI_TRIG2**	**GND**	PRST#	**PXI_STAR**	PXI_CLK10	**GND**
16	NC	**PXI_TRIG1**	PXI_TRIG0	DEG#	**GND**	PXI_TRIG7	**GND**
15	NC	PXI_BRSVA15	**GND**	FAL#	**PXI_LBL6**	**PXI_LBR6**	**GND**
14	NC	AD[35]	AD[34]	AD[33]	**GND**	AD[32]	**GND**
13	NC	AD[38]	**GND**		AD[37]	AD[36]	**GND**
12	NC	AD[42]	AD[41]	AD[40]	**GND**	AD[39]	**GND**
11	NC	AD[45]	**GND**		AD[44]	AD[43]	**GND**
10	NC	AD[49]	AD[48]	AD[47]	**GND**	AD[46]	**GND**
9	NC	AD[52]	**GND**		AD[51]	AD[50]	**GND**
8	NC	AD[56]	AD[55]	AD[54]	**GND**	AD[53]	**GND**
7	NC	AD[59]	**GND**		AD[58]	AD[57]	**GND**
6	NC	AD[63]	AD[62]	AD[61]	**GND**	AD[60]	**GND**
5	NC	C/BE[5]#]	**GND**		C/BE[4]#	PAR64]	**GND**
4	NC		PXI_BBRSVB4	C/BE[7]#	**GND**	C/BE[6]#	**GND**
3	NC	**PXI_LBR7**	**GND**	**PXI_LBR8**	**PXI_LBR9**	**PXI_LBR10**	**GND**
2	NC	**PXI_LBR11**	**PXI_LBR12**	SYSEN#	**PXI_LBL7**	**PXI_LBL8**	**GND**
1	NC	**PXI_LBL9**	**GND**	**PXI_LBL10**	**PXI_LBL11**	**PXI_LBL12**	**GND**

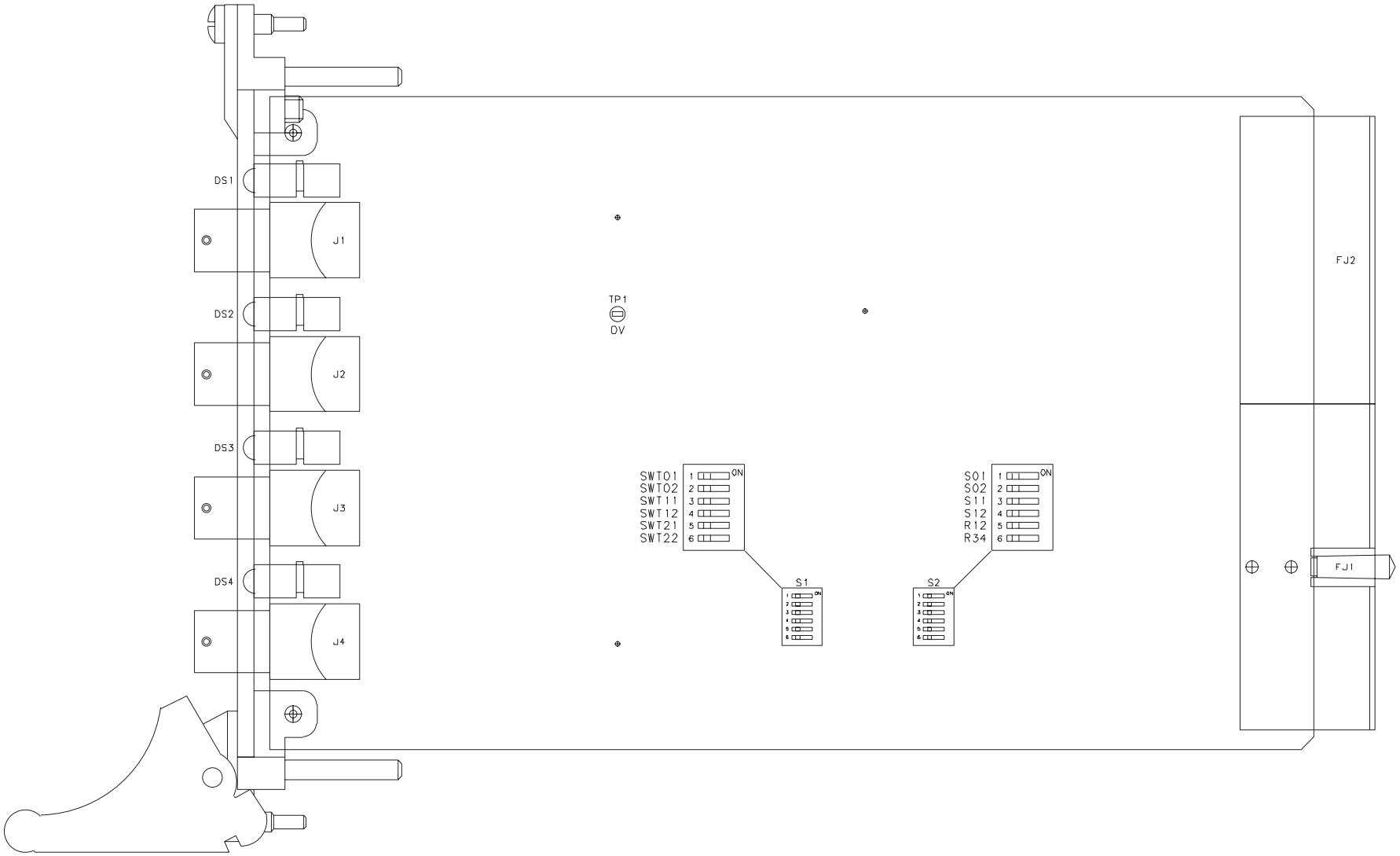


TRIGGER SYNCHRONISATION

Appendix

CONFIGURATION DRAWING

EQUIPMENT DRAWING



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ADAS électronique

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PLAN DE CONFIGURATION

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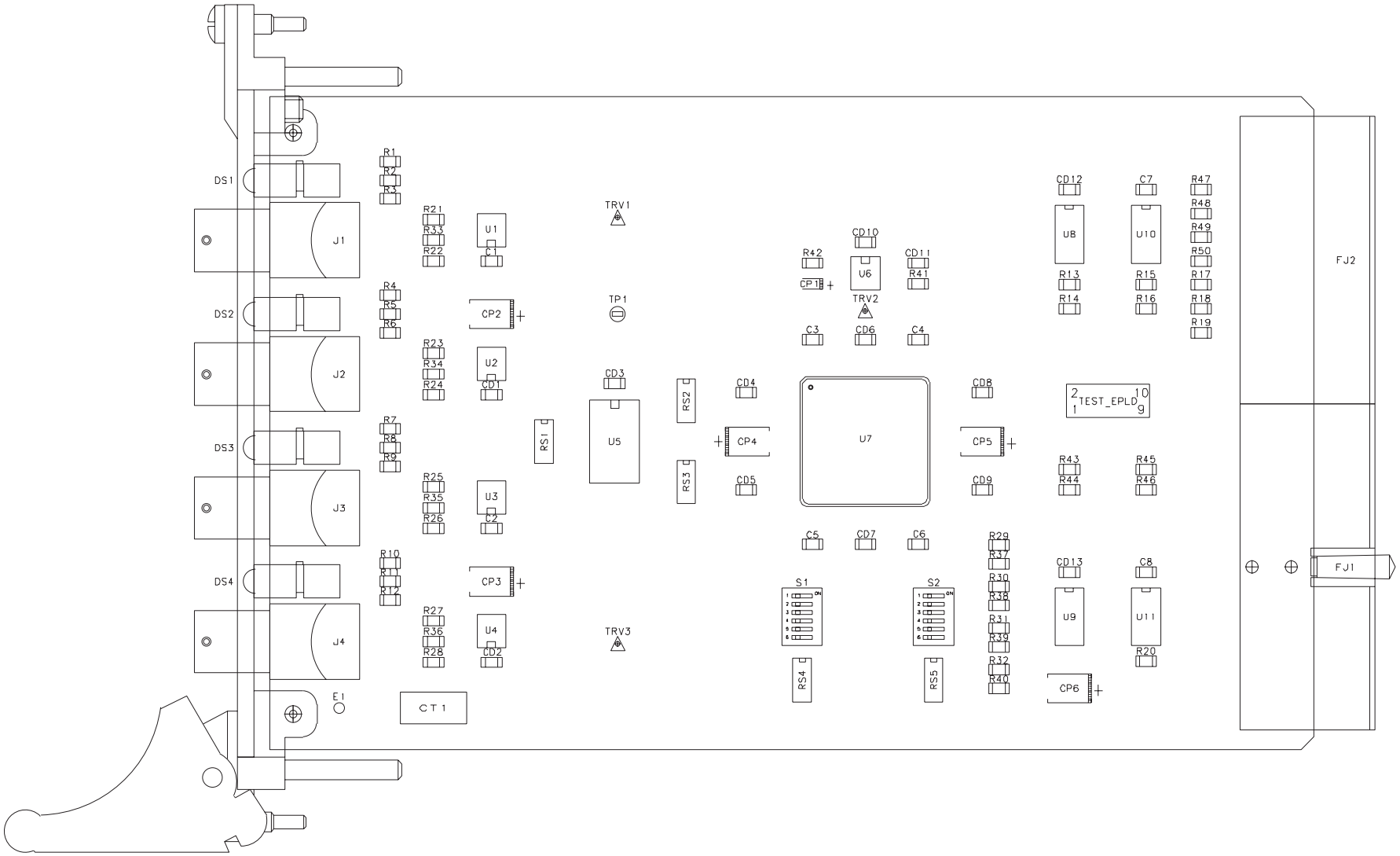

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