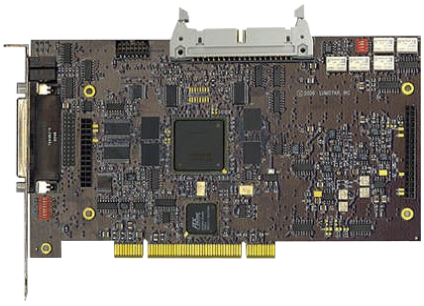
FS20/30

20 OR 30 MBPS FRAME SYNCHRONIZER



DESCRIPTION

The **FS20/30** Multi-function PCM Decommutator offers PCM decom, PCM simulator, IRIG time code reader/generator, and optional bit synchronizer in a single short PCI card slot. The simulator, decommutator, time code reader and time code generator are achieved on the board and the bit synchronizer is achieved through an optional low-profile daughterboard.
The IRIG Time Code Reader and Generator operate with IRIG A, B, or G time codes (in accordance with the IRIG Time Code Standards).
Both reader and generator are capable of operating at ½, 1, and 2 times the normal rate.

KEY FEATURES

- PCI Multifunction PCM Decommutator including
  - PCM Simulator with pre-mod filtering and BERT generating capability
  - PCM Simulator or BERT generating modes
  - PCM Decommutator with BERT reading capability
  - IRIG Time Code Reader and IRIG Time Code Generator
- FS10/20/30 Bit Synchronizer Daughterboard - Optional (10, 20 or 30 Mbps)
- CVSD Voice, h.261 Video and IRIG Chapter 8 Decoding through LDPS-Pro Software
- Short PCI Board only 7.55 inches long

SPECIFICATIONS

PCM Decommutator

Input Data Rate	64 bps to 20 or 30 Mbps (to define on order)
Input Signals	NRZ-L data & 0 degree clock
Input Levels	Single-ended TTL and RS-422
Word Length (VWL)	Variable from 3 to 32 bits per word on a word-by-word basis
CRC checker	CRC16/CCITT
Minor Frame Length	2 to 65,536 words per minor frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first (word-by-word basis)
Frame Sync Pattern	Up to 64 bits (any pattern with don't care bits (X) may be used)
Frame Sync Location	Beginning or end of the frame
Frame Sync Strategy	Adaptive mode (search-lock-verify) & burst mode (search-lock)
Sync Error Tolerance	0 to 15 bits (selectable)
Sync Slip Window	1, 3, 5, 7 bits wide (selectable)
Data Polarity	Normal, inverted or automatic
Sub-Frame Sync	FCC (FAC), SFID or URC (optional)
URC Location	Any 64 bits windows within the first minor frame not including the last bit in the minor frame
SFID Location	Any series of continguous bits not including the last bit in the minor frame

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PCM Simulator

Output	Data, 0 degree clock & minor strobes
Output Levels TTL, 422	Single-ended TTL or RS-422 levels ; On PCM Data and Clock
Base-band Output Level	400 mV to 8 V p-p adjustable
Base-band Pre-mod Filter	16 Selectable ; 5-pole Butterworth
Output Data Rate	64 bps to 20 Mbps (or 30 Mbps) for NRZ code ; 64 bps to 10 Mbps (or 15 Mbps) for other codes
PCM codes	NRZ-L/M/S, BIΦ-L/M/S, DM-M/S, M2, RNRZ-L (2^{11}, 2^{15}, -1)
Word Length	Variable from 3 to 16 bits per words on a word-per-word basis
CRC Generator	CRC16/CCITT
Minor Frame Length	2 to 32,767 words per minor frame
Major Frame Length	Up to 4.096 minor frames per major frame
Bit Order	MSB or LSB-first on a word-by-word basis
Frame Sync Pattern	Fully programmable
Sub-Frame Sync	Fully programmable

IRIG Reader/Generator

Time Reader Input Format	IRIG A, B or G
Time reader rate	$^1/_2$, 1 or 2 times normal rates
Input signal levels	1 V p-p nominal
Latency	2 µsec (maximum)
Data Outputs	Automatic time tags for PCM data blocks (time accessible in register space)
Time Generator Output	IRIG A, B, or G
Time generator Rate	$^1/_2$, 1 or 2 times normal rates

Environmental

Operating Temperature	10 to 50°C
Operating Humidity	10% to 90% Non-Condensing
Special Handling	Standard EDS methods required
Storage	Packaging must prevent contact with moisture and contaminants

Power Requirements

5 v	850 ma
-12 v	120 ma
+ 12 V	30 ma

ORDERING INFORMATION

FS20	20 mbps frame synchronizer
FS30	30 mbps frame synchronizer

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