A-664
ARINC-664 BOARD

DESCRIPTION

High performance intelligent PCI board offering full function test, simulation, monitoring and analyser functions for **ARINC-664** (Avionics Full Duplex Switched Ethernet) networks.

It's unique on board processing capability, memory resources, customised **ARINC-664** MACs and IRIG-B time code decoder/ generator gives **ARINC-664** users unparalleled features for the most demanding ARINC-664 applications.

The ARINC-664 board provides two **ARINC-664** ports being configured as two single or one dual redundant ports each implementing a 10/100Mbit Full Duplex Ethernet interface.

KEY FEATURES

- Two advanced 600 MHz XSCALE Processors on board
- Designed for applications such as:
  - Test & Verification of 'End Systems'
  - 'Switch' Testing
  - Monitoring of traffic between 'End Systems' & 'Switch'
  - Inter Switch Traffic Analysis
  - Multi Stream High Level System Integration
- Programmable Ports - Traffic Simulator and Receiver/Monitor Concurrently Synchronized Timing across Multiple Modules
- Magali driver interface

SPECIFICATIONS

Technical Data

System Interface	PCIbus Master & Slave
Processors:	Two 32-bit, 600MHz RISC Processors
Memory	64 MBytes Global RAM, 64 MBytes ASP RAM
Encoder/Decoder	Two ARINC-664 specific Ethernet MAC's Inter Frame Gap generation and measurement with 40 nsec resolution
Time Tagging	46 bit absolute IRIG-B Time with 1µsec resolution Inter Frame Gap generation and measurement with 40 nsec resolution
Physical bus interface	Two full duplex ARINC-664 ports configurable to one dual-redundant ARINC-664 port
Connector	PCI back plane connector. • 2 x 8 way RJ45 connectors, one per ARINC-664 port • 1 x 15 way DSUB connector (female) for Time Code and Trigger I/O
Dimensions	175 x 107 mm "short length" Standard PCI Format
Power Consumption	Typical 7 Watts (operating)

Environmental

Operating Temp. Range	Standard: 0°C...+55°C ambient. Extended: -15°C...+60°C ambient Extended –40°C... +85°C ambient
Storage Temp	-40°C ...+ 85°C ambient
Humidity	0 to 95% non-condensing

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Traffic Generation

- Programmable Timing & Sequencing of Frames
- Physical Error Injection - CRC, Gap, Size, Alignment
- Logical Error Injection on Layers 2, 3, 4
- Timing Error Injection - Violation of Bandwidth Allocation Gap (BAG)
- Autonomous Dynamic Data Generation
- UDP Port Simulation with Traffic Shaping & Sequence Numbering
- On-board support for sampling and queuing ports

UDP/VL Receive Mode

- VL oriented Filtering
- Second Level Filtering on Generic Frame Parameter
- Time Stamping of Received Packets with extended IRIG-B time code (1µs)
- Physical Error detection, Frame Level - CRC, Gap, Size and Alignment
- ARINC-664 Specific Error Detection
    - Traffic Shaping Verification
    - Verification of MAC, IP and UDP Headers
    - VL oriented Integrity Checking

Chronological Receive Mode

- VL Orientated Receive and Filtering
- Second level filtering on Generic Frame Parameters
- Chronological Monitor with Time Stamping to 1µs
- Massive on-board Monitor Buffer
- Inter frame Gap time measurements with 40 nsec resolution
- Comprehensive Triggering / Filtering / Capturing
- Programmable Data Capture Modes - Trace after Trigger & Recording
- Physical Error Detection - CRC, Gap, Size and Alignment
- ARINC-664 Specific Error Detection

Application Support Processor

- IP and UDP layer of the ARINC-664 protocol
- Driver Software Execution on the board
- Dynamic Data Generation
- Loop / Pollution between Rx and Tx port
- Automatic Test Sequence Generation
- Program using Real Time operating systems

IRIG-B Time Code Decoder

An on board IRIG-B Time Code decoder and generator allows synchronisation of multiple ARINC-664 ports using multiple API-FDX-2 modules. Modules can be synchronised using an external IRIG-B time source or the on-board Time code generator of one module as the reference for accurate correlation of data across multiple ARINC-664 ports.

Physical Bus Interface

- Customized Media Access Controllers (MAC's) implemented in FPGA optimised for ARINC-664
- 2 MByte Transmit / Receive Burst Buffer
- Physical Interface and Magnetics (COTS)
- 8-socket Network Interface connectors - RJ45
- Trigger, Strobe and Time Code I/O connector

ORDERING INFORMATION

MAG-300/A_A664/2	2 ARINC-664 ports—IRIG-B input time

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